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EXAMINER	
BORROMEO, JUANITO C	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/567,176	EVOY ET AL.	
	Examiner	Art Unit	
	JUANITO C. BORROMEO	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 4, 8 – 11, 22 – 25, 26, 27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg et al. (US Pat. No. 5598442), hereinafter referred to as Gregg' 442 in view of Bentz et al. (US Pat. No. 6363441), hereinafter referred to as Bentz' 441.

Referring to claim 1, Gregg' 442 discloses a data communication arrangement, comprising:

a transmit module (Figure 1, Serializer 46) adapted to convert parallel data words into a plurality of serial data streams (Figure 1, Element 46), each of which is carried by a data-carrying line (Figure 1, Lines 0 - 3); and

a receive module (Figure 2, Receiving module comprising 54, 56, 58, or 75) adapted to collect, for each data-carrying line, data carried from the transmit module by the data-carrying lines, and adapted to detect (Figure 2, Element 54) therein a frequency compensation code (Column 4, Lines 27 - 30) and, the receiving module adapted to align (Figure 2, Element 54) the data carried from the transmit module in response to the flag.

Gregg does not explicitly discloses a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

Bentz' 441 discloses a "timing controller 470 issues select signals to MUX 490 that cause the information in staging memory 475 to empty sequentially, ensuring information parallelly loaded at the particular time in staging memory 475 is unloaded before information loaded in staging memory 475 at a later time. In this example, time dependency maintenance system and method 400 ensures that parallel time dependencies are maintained on a first in first out (FIFO) basis between information parallelly loaded at one time period and information parallelly loaded at another time period.", col. 6, lines 38-48.

Thus, Bentz' 441 discloses a plurality of first in first out buffers (FIFOs) (time dependencies are maintained in a FIFO. In some embodiment, staing memory 475 comprises two columns thus has plurality of FIFO, col. 6, lines 45 - 52), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status (a representative bit to track timing dependencies associated with information, abstract and col. 6, lines 38-48) for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Bentz' 441 before him or her, to modify the

sync buffer 43 of Gregg to include the FIFO of Bentz' 441 because Bentz' 441's FIFO is use to maintain time dependent information.

The suggestion/motivation for doing so would have been to buffer data that have been skewed from conversion in order to facilitate utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information for a cache memory, as disclosed by Bentz' 441.

Therefore, it would have been obvious to combine Bentz' 441 with Gregg to obtain the invention as specified in the instant claim.

As to claim 2, Gregg' 442 discloses the data communication arrangement according to claim 1, wherein the receive module continuously checks alignment between the serial data streams and autonomously corrects alignment (Figure 3, Element 68) between the serial data streams (Column 4, Lines 27 - 35).

As to claim 3, Gregg' 442 discloses the data communication arrangement according to claim 1, wherein the receive module includes a retraining sequence delay circuit (Column 4, Lines 33 - 35) adapted to delay a retraining sequence request and provide a retry data transmit request (Column 4, Lines 39 - 40) in response to the frequency compensation codes to mitigate skew-caused re-training and configuration sequences.

As to claim 4, Gregg' 442 discloses the data communication arrangement according to claim 1, wherein the frequency compensation code is a Skip code (Figure 3, Desirializer 60).

Referring to claim 8, Gregg' 442 discloses a data communication arrangement, comprising:

a parallel word storage circuit (Figure 1) having a plurality of parallel to serial conversion modules (Figure 1, Serializer), each parallel to serial conversion module adapted to serially transmit a portion of the data from the parallel word storage circuit, each portion of data transmitted with an embedded frequency compensation code (Column 4, Lines 27 - 30); and

an alignment storage circuit (Figure 3) having a plurality of serial to parallel conversion modules (Figure 2), each serial to parallel conversion module adapted to receive the portions of data from the parallel word storage circuit, the alignment storage circuit adapted to provide an alignment detection signal (Figure 3, Element 68) to a data shift circuit in response to null character for each buffer, and adaptively shift (Figure 3, signal 69) the parallel data output from the portions of data in response to the alignment detection signal.

However, Gregg does not explicitly disclose each serial to parallel conversion module connected in parallel to a FIFO. At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the Sync buffer of Gregg to include a

FIFO. The suggestion/motivation for doing so would have been to temporarily store data streams as it is common and well known in the art of I/O.

Furthermore, Gregg does not explicitly discloses a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

Bentz' 441 discloses a "timing controller 470 issues select signals to MUX 490 that cause the information in staging memory 475 to empty sequentially, ensuring information parallelly loaded at the particular time in staging memory 475 is unloaded before information loaded in staging memory 475 at a later time. In this example, time dependency maintenance system and method 400 ensures that parallel time dependencies are maintained on a first in first out (FIFO) basis between information parallelly loaded at one time period and information parallelly loaded at another time period.", col. 6, lines 38-48.

Thus, Bentz' 441 discloses a plurality of first in first out buffers (FIFOs) (time dependencies are maintained in a FIFO. In some embodiment, staing memory 475 comprises two columns thus has plurality of FIFO, col. 6, lines 45 - 52), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status (a representative bit to track timing dependencies associated with information, abstract and col. 6, lines 38-48) for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Bentz' 441 before him or her, to modify the sync buffer 43 of Gregg to include the FIFO of Bentz' 441 because Bentz' 441's FIFO is use to maintain time dependent information.

The suggestion/motivation for doing so would have been to buffer data that have been skewed from conversion in order to facilitate utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information for a cache memory, as disclosed by Bentz' 441.

Therefore, it would have been obvious to combine Bentz' 441 with Gregg to obtain the invention as specified in the instant claim.

As to claim 9, Gregg' 422 discloses the data communication arrangement according to claim 8, wherein the alignment storage circuit includes a retraining sequence delay (Column 4, Lines 33 - 35) module adapted to delay a retraining sequence request and provide a retry data transmit request (Column 4, Lines 39 - 40) in response to the frequency compensation code.

As to claim 10, Gregg' 422 discloses the data communication arrangement according to claim 8, wherein the frequency compensation code is a Skip code (Figure 3, Desirializer 60).

As to claim 11, Gregg does not explicitly disclose wherein the SKIP codes are dropped and not placed into the FIFO. However, At the time of the invention, it would have been obvious to one of ordinary skill in art to modify the teachings of Gregg to include dropping unwanted code and place the rest of the data into a FIFO since this practice is well known and common in the art of I/O and networking to sync data streams with different frequencies (see pertinent art in the conclusion section).

Claims 22 – 25 recite the corresponding limitations of claim 1 – 4. Therefore, they are rejected accordingly.

Referring to claim 26, Gregg' 442 discloses a data communication arrangement, comprising:

a parallel circuit providing (Figure 1, Serializer) data symbols (output streams from element 46, Figure 1) in serial form on a plurality of data lines, at least some of the data symbols including codes useful for frequency compensation (Column 4, Lines 27 - 30); and an alignment circuit (Figure 1, Elements 54) adapted to respond to the codes by aligning the data symbols and by removing the codes.

Gregg does not explicitly discloses a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

Bentz' 441 discloses a "timing controller 470 issues select signals to MUX 490 that cause the information in staging memory 475 to empty sequentially, ensuring information parallelly loaded at the particular time in staging memory 475 is unloaded before information loaded in staging memory 475 at a later time. In this example, time dependency maintenance system and method 400 ensures that parallel time dependencies are maintained on a first in first out (FIFO) basis between information parallelly loaded at one time period and information parallelly loaded at another time period.", col. 6, lines 38-48.

Thus, Bentz' 441 discloses a plurality of first in first out buffers (FIFOs) (time dependencies are maintained in a FIFO. In some embodiment, staing memory 475 comprises two columns thus has plurality of FIFO, col. 6, lines 45 - 52), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status (a representative bit to track timing dependencies associated with information, abstract and col. 6, lines 38-48) for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Bentz' 441 before him or her, to modify the sync buffer 43 of Gregg to include the FIFO of Bentz' 441 because Bentz' 441's FIFO is use to maintain time dependent information.

The suggestion/motivation for doing so would have been to buffer data that have been skewed from conversion in order to facilitate utilization of parallel and sequential

graphics processing and communication hardware in an effective and efficient manner to support retrieval of information for a cache memory, as disclosed by Bentz' 441.

Therefore, it would have been obvious to combine Bentz' 441 with Gregg to obtain the invention as specified in the instant claim.

As to claim 27, Gregg' 442 discloses the data communication arrangement according to claim 26, wherein the alignment circuit includes a retraining sequence delay module (Column 4, Lines 33 - 35) adapted to delay a retraining sequence request (Column 4, Lines 39 - 40) and provide a retry data transmit request in response to the codes.

As to claim 29, Gregg' 442 discloses the data communication arrangement according to claim 26, wherein the symbols include clock information (Figure 1, signal 44).

As to claim 30, Gregg' 442 discloses the data communication arrangement according to claim 26, wherein the codes are Skip codes (Figure 3, Desirializer 60).

Claims 5 - 7, 28, and 31 - 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg' 442, in view of Bentz' 441 and in further view of Imanishi (US Pat. No. 5974055).

As to claim 5, Gregg does not explicitly disclose the receive module includes at least one shift register adapted to shift the serial data stream by at least one bit in response to the frequency compensation code.

However, Imanishi discloses the receive module includes at least one shift register (Figure 12, Shift Reg. 47) adapted to shift the serial data stream by at least one bit in response to the frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Imanishi before him or her, to modify the Sync buffer of Gregg to include the shift register of Imanishi.

The suggestion/motivation for doing so would have been to improve design flexibility.

Therefore, it would have been obvious to combine Imanishi with Gregg to obtain the invention as specified in the instant claim(s).

As to claim 6, Gregg does not explicitly disclose wherein the receive module includes at least one bit-shift pointer adapted to shift the serial data by at least one bit in response to the frequency compensation code.

However, Imanishi discloses at least one bit-shift pointer (Figure 12, Reg. 421) adapted to shift the serial data by at least one bit in response to the frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Imanishi before him or her, to modify the Sync buffer of Gregg to include the shift register of Imanishi.

The suggestion/motivation for doing so would have been to improve design flexibility.

As to claim 7, Gregg does not explicitly disclose wherein the receive module includes a direction indicator adapted to provide an indication of the shift direction for the bit-shift pointer.

However, Imanishi discloses a direction indicator adapted to provide an indication (Figure 12, Element 42) of the shift direction for the bit-shift pointer.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Imanishi before him or her, to modify the Sync buffer of Gregg to include the shift register of Imanishi.

The suggestion/motivation for doing so would have been to improve design flexibility.

Claims 28 and 31 recites the corresponding limitations of claims 5 and 6. Therefore, they are rejected accordingly.

Referring to claim 32, Gregg discloses a method for de-skewing data, comprising:

converting parallel data (Figure 1, sync buffer) into a plurality of serial bit-streams;

inserting (Figure 2, self timer) frequency compensation codes into at least one of the bit-streams;

transmitting the plurality of serial bit-streams (Figure 1, Serializer) over a plurality of parallel byte lanes, the parallel byte lanes susceptible to data skewing;

receiving (Figure 2) the plurality of serial bit-streams;

Gregg does not explicitly disclose:

performing a one-bit shift of the at least one of the bit-streams in response to the flag; and

dropping the frequency compensation codes from the at least one of the bit-streams before converting the plurality of serial bit-streams back into parallel data.

However, Imanishi discloses the method of performing a one-bit shift of the at least one of the bit-streams in response to the flag (Figure 12, Shift Reg. 47).

Therefore, it would have been obvious to combine Bentz' 441 with Gregg to obtain the invention as specified in the instant claim.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Imanishi before him or her, to modify the Sync buffer of Gregg to include the shift register of Imanishi.

The suggestion/motivation for doing so would have been to improve design flexibility.

In addition, At the time of the invention, it would have been obvious to one of ordinary skill in art to modify the teachings of Gregg to include dropping unwanted code before converting the plurality of serial bit-streams back into parallel data since this

practice is well known and common in the art of I/O and networking in order to sync data streams with different frequencies (see pertinent art in the conclusion section).

Furthermore, Gregg does not explicitly discloses a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

Bentz' 441 discloses a "timing controller 470 issues select signals to MUX 490 that cause the information in staging memory 475 to empty sequentially, ensuring information parallelly loaded at the particular time in staging memory 475 is unloaded before information loaded in staging memory 475 at a later time. In this example, time dependency maintenance system and method 400 ensures that parallel time dependencies are maintained on a first in first out (FIFO) basis between information parallelly loaded at one time period and information parallelly loaded at another time period.", col. 6, lines 38-48.

Thus, Bentz' 441 discloses a plurality of first in first out buffers (FIFOs) (time dependencies are maintained in a FIFO. In some embodiment, staing memory 475 comprises two columns thus has plurality of FIFO, col. 6, lines 45 - 52), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status (a representative bit to track timing dependencies associated with information, abstract and col. 6, lines 38-48) for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Bentz' 441 before him or her, to modify the sync buffer 43 of Gregg to include the FIFO of Bentz' 441 because Bentz' 441's FIFO is use to maintain time dependent information.

The suggestion/motivation for doing so would have been to buffer data that have been skewed from conversion in order to facilitate utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information for a cache memory, as disclosed by Bentz' 441.

As to claim 33, Imanishi discloses determining a shift direction (Figure 6, element 41) before performing the one-bit shift.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Imanishi before him or her, to modify the Sync buffer of Gregg to include the shift register of Imanishi.

The suggestion/motivation for doing so would have been to improve design flexibility.

As to claim 34, Imanishi discloses determining a bit-count before performing a plurality of one-bit shifts (Figure 6, element 44), the number of shifts equal to the determined bit-count.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Imanishi before him or her, to modify the Sync buffer of Gregg to include the shift register of Imanishi.

The suggestion/motivation for doing so would have been to improve design flexibility.

As to claim 35, Gregg discloses wherein the frequency compensation codes are Skip codes (Figure 3, Desirializer 60).

Claims 12 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg' 442 in view of Wakeman et al. (US Pat. No. 5790786), hereinafter referred to as Wakeman' 786, in further view of Bentz' 441 .

Referring to claim 12, Gregg' 422 discloses a receiver comprising:

an alignment storage circuit having a plurality of serial to parallel conversion modules (Figure 1).

However , Gregg does not explicitly disclose each serial to parallel conversion module adapted to connect to a PCI Express bus line and convert a serial bit stream to parallel data words, and each serial to parallel conversion module connected in parallel to a FIFO, the alignment storage circuit adapted to provide an alignment detection signal to a data shift circuit in response to the flag for each FIFO, and adaptively shift

the parallel data output from the serial bit stream in each serial to parallel conversion module in response to the alignment detection signal.

Wakeman discloses each serial to parallel conversion module adapted to connect to a PCI Express bus line (Figure 1B, Systme bus 116) and convert a serial bit stream to parallel data words, and each serial to parallel conversion module connected in parallel to a FIFO (Figure 1B, Transmit FIFO), the alignment storage circuit adapted to provide an alignment detection signal to a data shift circuit (Column 3, Lines 19 - 25) in response to detection of a frequency compensation code for each serial bit-stream, and adaptively shift the parallel data output from the serial bit stream in each serial to parallel conversion module in response to the alignment detection signal (Column 3, Lines 25 - 28).

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Wakeman before him or her, to modify the Sync buffer of Gregg to include multi access control circuit of Wakeman.

The suggestion/motivation for doing so would have been to transmit data via a multi access network.

Therefore, it would have been obvious to combine Wakeman with Gregg to obtain the invention as specified in the instant claim(s).

As to claim 13, Gregg discloses wherein the alignment storage circuit continuously checks alignment between the plurality of serial to parallel conversion

modules and autonomously corrects alignment between the plurality of serial to parallel conversion modules (Column 4, Lines 27 - 35).

Furthermore, Gregg does not explicitly discloses a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

Bentz' 441 discloses a "timing controller 470 issues select signals to MUX 490 that cause the information in staging memory 475 to empty sequentially, ensuring information parallelly loaded at the particular time in staging memory 475 is unloaded before information loaded in staging memory 475 at a later time. In this example, time dependency maintenance system and method 400 ensures that parallel time dependencies are maintained on a first in first out (FIFO) basis between information parallelly loaded at one time period and information parallelly loaded at another time period.", col. 6, lines 38-48.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Bentz' 441 before him or her, to modify the sync buffer 43 of Gregg to include the FIFO of Bentz' 441 because Bentz' 441's FIFO is use to maintain time dependent information.

The suggestion/motivation for doing so would have been to buffer data that have been skewed from conversion in order to facilitate utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information for a cache memory, as disclosed by Bentz' 441.

Therefore, it would have been obvious to combine Bentz' 441 with Gregg to obtain the invention as specified in the instant claim.

As to claim 14, Gregg discloses wherein the alignment storage circuit includes a retraining sequence delay module (Column 4, Lines 33 - 35) adapted to delay a retraining sequence request (Column 4, Lines 39 - 40) and provide a retry data transmit request in response to the frequency compensation code.

As to claim 15, Gregg discloses wherein the alignment storage circuit uses the frequency compensation codes to automatically correct synchronization errors (Column 4, Lines 15 - 25) between the plurality of serial to parallel conversion modules.

As to claim 16, Wakeman discloses a shift register (Figure 3B, Shift register 335) adapted to shift the serial bit stream by at least one bit in response to the alignment detection signal. At the time of the invention, it would have been obvious to one of ordinary skill in the art to add a shift register to Gregg's system for sequencing purposes as known in the art.

Claims 17 and 18 recite the corresponding limitations of claims 6 and 7. Therefore, they are rejected accordingly.

Claims 19 and 20 recites the corresponding limitations of claims 12 and 13. Therefore, they are rejected accordingly.

As to claim 21, Wakeman disclose wherein the serial data is transmitted over a fast Ethernet connection (Column 1, line 9).

Response to Arguments

Applicant's arguments filed 5/1/2009 have been fully considered but they are not persuasive.

Applicant's invention corrects errors in a data signals transmitted on multiple serial byte lanes through a bit dedicated to a flag indicating alignment status for the data collected in the FIFO.

Gregg discloses a self-timed parallel/serial data communication channel. However, Gregg does not specifically disclose how to deal with skew errors during conversion between parallel to serial in the data communication channels.

On the other hand, Bentz discloses timing controller having dependency memory, selection serialization components and reordering component for maintaining time dependencies in conversions between sequential and parallel operation using stating memory.

So how does Bentz's system discloses a bit dedicated to a flag indicating alignment status for the data collected in the FIFO?

Bentz' 441 discloses a "timing controller 470 issues select signals to MUX 490 that cause the information in staging memory 475 to empty sequentially, ensuring information parallelly loaded at the particular time in staging memory 475 is unloaded

before information loaded in staging memory 475 at a later time. In this example, time dependency maintenance system and method 400 ensures that parallel time dependencies are maintained on a first in first out (FIFO) basis between information parallelly loaded at one time period and information parallelly loaded at another time period.", col. 6, lines 38-48.

The timing controller utilizes a representative bit to track timing dependencies associated with information (analogous to a bit dedicated to a flag indicating alignment status) and ensures the information is communicated and processed in an order that preserves the timing dependencies as the information is converted from parallel or parallel to serial operation (see abstract).

In summary, Bentz' 441 discloses a plurality of first in first out buffers (FIFOs) (time dependencies are maintained in a FIFO. In some embodiment, staing memory 475 comprises two columns thus has plurality of FIFO, col. 6, lines 45 - 52), each FIFO coupled to a data-carrying line; and wherein each FIFO comprises a bit dedicated to a flag indicating alignment status (a representative bit to track timing dependencies associated with information, abstract and col. 6, lines 38-48) for the data collected in the FIFO, the flag is set in response to the detected frequency compensation code.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Gregg and Bentz' 441 before him or her, to modify the sync buffer 43 of Gregg to include the FIFO of Bentz' 441 because Bentz' 441's FIFO is use to maintain time dependent information.

The suggestion/motivation for doing so would have been to buffer data that have been skewed from conversion, to/from serial to/from parallel, in order to facilitate utilization of parallel and sequential graphics processing and communication hardware in an effective and efficient manner to support retrieval of information for a cache memory, as disclosed by Bentz' 441.

Therefore, it would have been obvious to combine Bentz' 441 with Gregg to obtain the invention as specified in the instant claim.

As such, Examiner respectfully maintains the 35 USC § 103 rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUANITO C. BORROMEO whose telephone number is (571) 270-1720. The examiner can normally be reached on Mon-Fri, 8:30 AM - 5:00 PM, ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571 272 4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Henry W.H. Tsai/
Supervisory Patent Examiner, Art Unit 2184